AMENDMENTS TO THE DRAWINGS

This Amendment is being transmitted together with a Transmittal of Drawing Correction including changes to FIGS. 4A and 4B. The Amendments overcome the objection to the drawings raised on page 4 of the Office Action. No new matter has been added.

REMARKS

In response to the Office Action dated January 9, 2007, Applicants respectfully request reconsideration. Claims 1-31 were pending in this application. Claims 14-31 have been cancelled, because they are subject to a restriction requirement. Claims 1 and 2 have been amended for the purposes of clarification only. New claims 32-35 have been added, with claims 32 and 33 being independent claims. Therefore, claims 1-13, and 32-35 are pending, with claims 1, 32, and 33 being independent claims.

ELECTION/RESTRICTION

Applicants acknowledge that in response to a request from the Examiner, as discussed in pages 2-4 of the office action, an election of claims 1-13, corresponding to Group 1, has been made. Accordingly, claims 14-31 have been cancelled.

DRAWINGS

The drawings are objected to because FIGS. 4A and 4B allegedly contain elements shown in color. Applicants have amended these drawings as shown in the Transmittal of Drawing Correction accompanying this Amendment. As amended, the drawings contain a black and white dotted fill pattern which complies with 37 CFR 1.121(d). Accordingly, Applicants request that the objection to the drawings be withdrawn.

CLAIM REJECTIONS UNDER 35 U.S.C §112

Claims 1 and 2 stand rejected under 35 U.S.C. §112, second paragraph, as allegedly being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicants regard as the invention. Applicants have amended claims 1 and 2 for purposes of clarification only. Applicants believe that these amendments adequately address the concerns of the Examiner, and that the claims satisfy the requirements of 35 U.S.C. §112, second paragraph.

Accordingly, Applicants respectfully request that the rejections of claims 1 and 2 under 35 U.S.C. §112 be withdrawn.

CLAIM REJECTIONS UNDER 35 U.S.C. §103(a)

Claims 1-13 stand rejected under 35 U.S.C. §103(a). In particular, claims 1, 2, 4, 6, 7 and 11-13 stand rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over Lesmeister (US Pat. No. 5,748,642). Applicants respectfully traverse this rejection.

Discussion Of Technology

The discussion provided herein is simply for purposes of background. It is not a characterization of the invention or of the cited art. It is not intended as a substitute for the Examiner's reading of the specification and of the cited art in their entireties. It does not limit the claims in any way, and does not replace a thorough reading of the claims.

The present application relates to test systems using multiple instruments and control of the instruments within the test system. The test system allows for independent construction of the instruments, while providing coordinated operation of the instruments. As described in the Background, one way to coordinate the operation of the instruments is by using a clock signal that is sent to all the instruments. For a test system that provides fast operation, the clock signal must have a high frequency. However, there is often a practical limit to the frequency of a reference clock that can be reliably fanned out to many instruments in a test system. Therefore, if the instruments of the test system are coordinated by a reference clock signal, the limit in the frequency of the clock signal that can reliably be fanned out to the instruments creates a practical limit on the speed of operation of the test system.

The present application describes an alternative method of coordinating the instruments that can be used for a test system that operates at a higher speed. A relatively low frequency reference clock is provided to the instruments, which then generate higher frequency local clocks for use within the instruments. To coordinate the operations of the instruments, messages

containing time values can be sent to the instruments. A time value can specify a time for execution of an operation relative to a local clock. If the local clocks of multiple instruments are synchronized, then high speed coordinated operation of the instruments can be achieved.

An example of such a test system is provided in the specification of the present application. As illustrated in FIG. 2, a semiconductor tester may include a computer work station 22, and a test head 24. (page 5, lines 29-31). The test head 24 houses multiple instrument cards 30. (page 5, line 31 – page 6, line 2). The instruments on instrument cards 30 may be digital or analog instruments. (page 6, line 19). Instrument 30a depicts a digital instrument. (FIG. 2; page 6, lines 19 - 21). The test system allows for independent construction of the instruments, while providing high speed coordinated operation of the instruments, as now described.

To enable high speed operation, a reference clock generator 34 can generate a reference clock RCLK that can be fanned out to the instruments. (FIG. 2; page 6, lines 4-6). As mentioned, there may be an upper limit to the frequency of RCLK that can be reliably fanned out to the instruments and RCLK has a frequency below this limit. For higher frequency operation of instruments, each instrument, such as channel card 30a may include a clock module 42. The clock module 42 may be programmed to generate one or more local clocks of a desired frequency from RCLK. (page 6, lines 24-26). The frequency of a local clock generated by clock module 42 can differ from the frequency of RCLK. For example, the frequency of a clock generated by clock module 42 may be higher than the frequency of RCLK, providing higher speed operation of the instrument. Each of the clocks generated by a clock module 42 can be used "locally", *i.e.*, within the instrument or board containing the clock generator. (page 6, line 26-28).

The test system is also configured to allow coordinated operation of the instruments. Instruments, such as instrument 30a, include an instrument synchronization link (ISL) interface 320a. (page 7, lines 19-20). ISL interface 320a allows pattern generator 46, which provides a sequence of commands that control the functional portion of the instrument 30a, to communicate with other instruments. (page 7, lines 12-14 and 20-21). For example, the pattern generator 46 may send commands to be executed by the functional circuitry of other instruments or receive status

information from other instruments. (page 7, lines 21-23). Each pattern generator may be programmed with commands for multiple instruments in the system to execute. (page 8, lines 9-10).

The operation of multiple instruments can then be coordinated in the following manner. The local clock signals can be synchronized. Time is tracked on each instrument using a local watch (page 8, lines 26-28). The timing of events of the various instruments can then be coordinated by reference to time as tracked by the local watches. (page 8, lines 29-30). For example, a first instrument may send a command to a second instrument (page 8, lines 29-31). The time of execution of that command may be specified relative to the local watch of the first instrument. (page 8, lines 31-32).

By establishing a common time reference, the signals that convey the commands or other messages do not need to be transmitted synchronously. (page 9, line 6-7). For example, a simple asynchronous communication link may be employed that relies on time values in the messages to control the timing of the events. (page 9, lines 7-9). In this manner, the test system provides coordinated operation of the instruments, and the instruments can still be independently constructed.

Discussion Of Lesmeister

Lesmeister discloses integrated circuit testers including several processing nodes, each generating or measuring one signal at each terminal of a device under test. (Abstract, col. 1, lines 21-28). The integrated circuit tester is designed in an attempt to solve a problem with the prior art of that time relating to limited node memory storage (col. 2, lines 18-21).

As discussed by Lesmeister, an integrated circuit test is organized into a set of successive time segments, called test cycles (col. 1, lines 24-25). Generally a tester stores one command in each node memory for each cycle of testing. (col. 1., lines 47-48). However, the length of command sequences needed for the tests have become so large that they exceed the practical storage size of a node memory. (col. 1, lines 48-56). Therefore, Lesmeister is attempting to provide an

integrated circuit tester that can perform long, high speed integrated circuit tests with great flexibility in timing selection, without requiring large node memories. (col. 2, lines 18-21).

FIG. 1 is a block diagram of a parallel processing integrated circuit tester as disclosed by Lesmeister. (col. 3, lines 11-13). The tester 10 includes several processing nodes 14. (col. 3, line 60). Each node may be linked to the device under test (DUT) via a conductor 16. (col. 3, line 62-64). The processing nodes 14 are interconnected by unidirectional transmission lines 18 and 19. (col. 4, lines 26-29; col. 4, lines 59-62). The tester 10 also includes a host interface 20, which provides a host computer 22 with access to the network via a bus 24. (col. 4, lines 30-33). A reference oscillator clock signal ROSC is produced by clock circuit 25 and provided to all nodes 14. (col. 4, lines 33-37).

FIG. 2 is a block diagram of a typical node 14 of the integrated circuit tester shown in FIG. 1. The node 14 includes network interface 30 for interfacing the node to the unidirectional incoming and outgoing serial transmission lines 18 and 19 (col. 4, lines 59-62) (col. 3, 14-15). The network interface 30 receives serial data and addresses via incoming transmission line 18. (col.5, lines 7-11). The network interface may forward data to local bus 31. (col. 5, lines 11-13). The network interface 30 also forwards the incoming serial data and addresses to the next node in the network via outgoing transmission line 19 (col. 5, lines 7-11). In this manner, the data is forwarded from one node to another, cycling through the node network.

As mentioned, Lesmeister attempts to resolve a problem with limited node memory storage (col. 2, lines 18-21). Accordingly, the node 14 includes a memory 34 for storing algorithmic instructions. (col. 5, lines 1, 3). The algorithmic instructions are used to generate a sequence of commands (col. 2, lines 31-35). Lesmeister asserts that the amount of memory needed to store algorithmic instructions for generating the command sequences is much smaller than the amount of memory needed to store the command sequences themselves. (col. 2, lines 41-45).

As shown in FIG. 2, the node 14 also includes a memory management unit 32. The memory management unit 32 determines whether the data received through the network interface 30

is addressed to memory 34 of node 14. If the memory 34 is being addressed, then the memory management unit 32 stores the data in memory 34. (col. 5, lines 12-15). Processing unit 36 then executes the instructions stored in memory 34. (col. 5, lines 3-5). Therefore, Lesmeister implies that if the memory 34 is not being addressed, the data received on the network interface 30 is not stored in the memory 34.

The node 14 also includes circuitry to help synchronize the operations of the nodes (col. 5, lines 62-64). The node 14 includes an oscillator 42, time formatter 38, and DUT interface circuit 40. (col. 5, lines 21-22, 62-64). The oscillator 42 produces a set of timing signals transmitted to the time formatter 38 and the network interface 30. (col. 5, lines 64-66). The timing signals also clock instruction processing by the processing unit 36 (col. 6, lines 2-4).

The timing signals are used to synchronize the operations of the nodes. The timing signals have the same frequency as the ROSC signal sent to all the nodes, though they may be time shifted relative to each other. (col. 5, line 66- col. 6, line 2). The timing signals produced by oscillator 42 in all of the nodes have the same phase relationship to the ROSC signal (col. 6, lines 8-11). Therefore, the timing signals of each node are in phase with similar signals in the other nodes (col. 6, lines 8-11). Because instruction processing is referenced to the timing signals, the activities of the nodes can be synchronized (col. 6, lines 11-13).

Claim 1 Is Not Obvious In View Of Lesmeister

The Office Action asserts that claim 1 is unpatentable in view of Lesmeister. Applicants respectfully disagree.

First, Applicants disagree with the characterization of Lesmeister set forth in the Office Action. The Office Action equates host interface 20 in FIG. 1 of Lesmeister with the claimed first instrument. (Office Action page 7). Applicants disagree with this assertion for at least two reasons.

First, the claimed first instrument comprises a first local clock generator. In contrast, Lesmeister does not disclose that host interface 20 comprises a local clock generator. The Office Action cites oscillator 42 in FIG. 2, and column 5, lines 62-64 of Lesmeister as providing the

claimed first local clock generator. However, the cited portion of Lesmeister specifies that oscillator 42 is included in each node 14. The reference contains no teaching or suggestion of an oscillator in the host interface 20. Because the host interface 20 does not comprise a first local clock generator, the host interface 20 cannot correspond to the claimed first instrument.

Second, the host interface 20 in FIG. 1 of Lesmeister also fails to correspond to the claimed first instrument because it lacks the claimed first control circuit. In particular, the claimed first instrument comprises a first control circuit storing programmed commands for the first instrument and a second instrument. The Office Action asserts that the description of Lesmeister at column 5, lines 1-5 corresponds to the claimed first control circuit. (Office Action page 7). However, the cited portion of Lesmeister describes the operation of instruction memory 34 and processing unit 36. This portion of Lesmeister is describing the configuration of a node 14, not the host interface 20. (col. 4, line 66 - col. 5, line 5). Therefore, the host interface 20 cannot correspond to the claimed first instrument because the host interface 20 does not comprise the claimed first local clock generator or the claimed first control circuit.

Next, Applicants disagree with the assertion in the Office Action that Lesmeister discloses a first control circuit meeting the limitations of claim 1. Claim 1 specifies that the first instrument comprises a first control circuit storing programmed commands for the first instrument and a second instrument. This limitation is not met by Lesmeister.

The Office Action cites to col. 5, lines 1-5 of Lesmeister as disclosing the claimed first control circuit. The cited portion of Lesmeister describes the operation of instruction memory 34 and processing unit 36. However, there is no disclosure in Lesmeister that the memory 34 or the processing unit 36 stores programmed commands for the first instrument and the second instrument. Rather, Lesmeister states that processing unit 36 executes the instruction stored in memory 34 to produce a sequence of commands controlling node operations (col. 5, lines 3-5). There is no teaching or suggestion that memory 34, or processing unit 36, stores programmed commands for the first instrument and a second instrument, as recited in claim 1.

Accordingly, claim 1 is not obvious from Lesmeister because making the modifications to Lesmeister suggested in the Office Action would not result in the claimed invention. In particular, even if one were to make the modifications to Lesmeister suggested in the Office Action, and

described more fully below, one would not achieve the claimed first control circuit. Lesmeister simply fails to teach or suggest the first control circuit as recited in claim 1. Accordingly, claim 1 is patentable over Lesmeister for at least this reason.

In addition to the differences highlighted above between the claimed invention and Lesmeister, the Office Action concedes that Lesmeister fails to explicitly disclose that the first control circuit is coupled to the network to provide the time value in the message and the second control circuit is coupled to the network to receive the time value at its input (Office Action page 8). However, the Office Action asserts that it would have been obvious to modify Lesmeister to meet this claim limitation. Applicants respectfully disagree.

It would not have been obvious to modify Lesmeister in the manner suggested by the Office Action because one of skill in the art would not be motivated to make the suggested modification without the benefit of Applicants' specification. Specifically, the Office Action states that the modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that doing so would have only required a rearranging of parts within the system of Lesmeister (Office Action page 8). However, this reasoning is improper. MPEP 2144.04(VI)(C) recites the principles that:

> "The mere fact that a worker in the art could rearrange the parts of the reference device to meet the terms of the claims...is not by itself sufficient to support a finding of obviousness. The prior art must provide a motivation or reason for the worker in the art, without the benefit of appellant's specification, to make the necessary changes in the reference device." (*citing Ex parte* Chicago Rawhide Mfg. Co., 223 USPQ 351, 353 (Bd. Pat. App. & Inter. 1984).

Lesmeister does not provide any motivation or reason to make the modification suggested in the Office Action. Therefore, even if the proposed modification would result in the claimed invention, which Applicants' have noted is not the case, the rejection of claim 1 under 35 U.S.C. 103(a) is improper because Lesmeister provides no motivation or reason to make the suggested modifications. Accordingly, Applicants respectfully request that the rejection of claim 1 under 35 U.S.C. § 103(a) be withdrawn.

Claims 2-13 depend directly or indirectly from independent claim 1, and are patentable for at least the same reasons. Accordingly, Applicants respectfully request that the rejections of claim 2-13 be withdrawn.

NEW CLAIMS

New claims 32-35 have been added to further define applicants' contribution to the art. Claims 32 and 33 are independent claims. No new matter has been added.

Claim 32 recites a test system. The test system comprises, *inter alia*, a first instrument of the plurality of instruments, the first instrument comprising a first control circuit storing programmed commands for the first instrument and the second instrument. The test system also comprises a second instrument comprising a second control circuit having an input and an output, the second control circuit asserting the output at a time based at least in part on a comparison of a time value provided at the input to the second control circuit to a time tracked by a second time tracking circuit.

Support for claim 32 can be found in the application as originally filed. For example, support can be found in FIGS. 2 and 3, and the corresponding portion of the specification, as well as the original claim set. Applicants believe that claim 32 is patentable over the prior art. The prior art does not disclose the claimed first instrument comprising a first control circuit storing programmed commands for the first instrument and the second instrument. The prior art also fails to disclose the claimed second control circuit asserting the output at a time based at least in part on a comparison of a time value provided at the input to the second control circuit to a time tracked by a second time tracking circuit. For at least these reasons, claim 32 is patentable over the prior art.

Claim 33 recites a test system. The test system comprises a reference clock generator providing a reference clock having a plurality of periods. The test system also comprises, *inter alia*, a first instrument comprising a first control circuit storing programmed commands for the first instrument and a second instrument. The test system further comprises a network between at least the first instrument and the second instrument, the network carrying a message during a first period

of the plurality of periods of the reference clock. The message includes a time value. The test system further comprises a second instrument comprising a second control circuit having an input and an output, the second control circuit asserting the output at a time specified by the time value, wherein the time value specifies a time during a second period of the reference clock.

Support for claim 33 can be found in the application as originally filed. For example, support can be found in FIGS. 2 and 3 and the corresponding description in the specification. Support can also be found in the specification at p. 9, lines 1-9.

Applicants believe that claim 33 is patentable over the prior art. The prior art fails to disclose the claimed first instrument comprising a first control circuit storing programmed commands for the first instrument and a second instrument. The prior art also fails to disclose a network between at least the first instrument and the second instrument, the network carrying a message during a first period of the plurality of periods of the reference clock, wherein the message includes a time value specifying a time during a second period of the reference clock. For at least these reasons, claim 33 is patentable over the prior art.

Claims 34 and 35 depend from claim 33 and are patentable for at least the same reasons.

In view of the above amendment, Applicants believe the pending application is in condition for allowance.

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